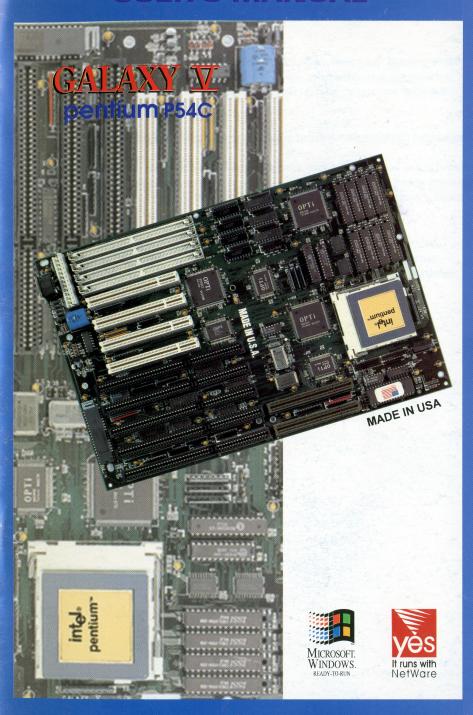
USER'S MANUAL



The OPTi 82C606 is a buffer/translation device used to translate 3.3V signal to 5.0V signal levels. This device buffers the CPU address bus to the ISA and VL address buses, the 82C546 memory data bus to the ISA data bus, the peripheral XD bus to the ISA SA and SD buses. It integrates a number of glue logic TTL devices, thus reducing the amount of TTL in the motherboard.

The OPTi 82C206 IPC provides two DMA controllers, two interrupt controllers, one timer/counter, and real-time clock in an industry standard single-chip solution for the peripherals attached to the PC/AT peripheral bus.

For more detailed features about the OPTi 82C822, 546, 547, 606, and 602 chipsets, please refer to Section 4 'Technical Information' under chipset overview.

1.2	Sp	ecif	ica	tio	ns

• CPU	Intel Pentium Processor
• SPEED	90 or 100 MHz
• PCI	4 PCI bus master slots
• VESA	2 VESA bus slots
• ISA	5 16-bit standard AT slots
• CACHE	Supports 64KB, 256KB and 512KB in either WB/WT mode
• DRAM	Four 72-pin SIMM sockets support 2MB up to 128MB of on board memory using 1/2/4/8/16/32 MB 72-pin DRAM Module.
• BIOS	AMI BIOS (w/ flash ROM support optional)
• SOCKET	On board Zif socket for CPU
• CHIPSET	OPTi 82C822, 82C546, 82C547, 82C606 and 82C206
OS Support	MS DOS, Windows, Windows NT, OS/2, Novell, SCO UNIX, and XENIX

Performance :

Processor Benchmarks		Intel Pentium 100 MHz	Intel Pentium 90 MHz	
Landmark	v3.0	3988.1	3493.8	
PowerMeter	v1.7	68.4	62.9	
PC Bench	v8.0	120.2	108.1	

P54C User's Manual

VL Bus ID2 Selects

NA 1814	Selection	JP23
10,030 00 00 00	ligh Speed Write Set for OWS	Open
Default	ligh Speed Write Set for 1WS	The same of the same of
	right speed write set for Tws	Ciose

2.5.8 82C546 Power Up Selections

JP13	JP14	Selection	2
Close	Close	ATCLK Selected as LCLK/5	rectal at
Open	Close	ATCLK Selected as LCLK/4	Default
Close	Open	ATCLK Selected as LCLK/3	Delaun
Open	Open	ATCLK Selected as LCLK/2	3 1 2 2 2 2 2

JP15	Selection	Ass. Abs.
Open	Slow AT Back to Back I/O Delay (3 AT Clocks Added)	Default
Close	Fast AT Back to Back I/O Delay (0 AT Clocks Added)	Delauit

JP18	Selection	2 (0.00)
Open	LDEV# Sampling Selected at End of First T2	Default
Close	LDEV# Sampling Selected at End of Second T2	Delauit

3.0 AMI BIOS Setup

CMOS SETUP PROCEDURE:

- 1. Power up your system.
- 2. Hit the **Del** key for several times while your system is checking its memory.
- 3. The system may ask you to press the F1 key.
- 4. The screen should then appear as follows:

